Confirmation No. 7635 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	VAN DE WAERDT	Examiner:	Cygiel, G.
Serial No.:	10/535,591	Group Art Unit:	2187
Filed:	May 19, 2005	Docket No.:	US020465US (NXPS.368PA)
Title:	USING A CACHE MISS PATTERN TO ADDRESS A STRIDE PREDICTION TABLE		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. § 41.37, in support of the Notice of Appeal filed March 9, 2011, and in response to the rejections of claims as set forth in the Final Office Action dated December 17, 2010, and the Advisory Action dated March 1, 2011.

Please charge Deposit Account No. 50-4019 (US020465US) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-4019 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-21 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated December 17, 2010.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an embodiment of the present invention is directed towards a method of data retrieval comprising the following steps. A first memory circuit, stride prediction table (SPT) that is indexed with cache line miss information, and cache memory circuit are provided. *See, e.g.*, Figure 6 and page 7:30-8:18. Instructions for accessing data within the first memory are executed. *Id.* A cache miss is detected, and accesses and updates to the SPT are allowed only in response to the detection of the cache miss. *Id.*

Commensurate with independent claim 11, an embodiment of the present invention is directed towards an apparatus comprising a stride prediction table (SPT) and a filter circuit for use with the SPT. *See, e.g.*, Figure 6 and page 7:30-8:3. The SPT is indexed with cache line miss information. *See, e.g.*, Figure 6 and page 8:19-29. The filter circuit prevents both accesses and updates to the SPT unless a cache miss is detected. *See, e.g.*, Figure 6 and page 7:30-8:18.

Commensurate with independent claim 17, an embodiment of the present invention is directed towards a method of data retrieval comprising the following steps. A first memory circuit, a stride prediction table (SPT) that is indexed with cache line miss information, and a cache memory circuit are provided. *See, e.g.*, Figure 6 and page 7:30-8:18. Instructions for accessing data within the first memory are executed, a cache miss is detected, and accesses to the SPT are restricted in response to detecting the cache miss. *See id.*, and page 8:19-29.

Commensurate with independent claim 21, an embodiment of the present invention is directed to a method of data retrieval. A first memory circuit and a single-ported SRAM memory are provided, the SRAM memory having a cache memory circuit and a stride prediction table (SPT) that is indexed with cache line miss information. *See, e.g.*, Figure 6 and page 7:30-8:29. In a filter circuit, an application stream having a plurality of access instructions for accessing data in the first memory circuit is received. *See, e.g.*, Figure 6 and page 8:4-12. Also in the filter circuit, and for each of the plurality of access instructions that are load access instructions, the cache memory is accessed to determine whether data at a memory location of the load access instruction is present within the cache, and a cache miss for the load access instruction is detected when the data is other than present within the cache. *Id.* Also in the filter circuit, accesses and updates to the SPT are restricted to only

load memory access instructions for which a cache miss is detected. *See, e.g.*, Figure 6 and page 8:4-18. In response to an update to the SPT indicative of one of said detected cache misses, instructions are executed to access the SPT and predict a cache miss. *Id.* In response to a predicted cache miss, the loading of a stream cache is controlled based upon the memory location of the load access instruction. *Id.*

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-2, 4-8, 10-14, 16-18 and 20 stand rejected under 35 U.S.C. § 102(b) over the Sherwood *et al.* ("Predictor-Directed Stream Buffers").

B. Claim 21 stands rejected under 35 U.S.C. § 103(a) over the Sherwood reference in view of Matas ("Memory 1997", Integrated Circuit Engineering Corporation).

C. Claims 3, 9, 15 and 19 stand rejected under 35 U.S.C. § 103(a) over the Sherwood reference in view of Handy ("The Cache Memory Book").

VII. Argument

Appellant believes that all rejections are improper for relying upon a mistaken interpretation of the primary Sherwood reference, upon which all rejections rely. In short, the Final Office Action mistakenly attributes portions of the Sherwood reference that discuss a "Markov prediction table," as instead pertaining to a stride table (the asserted "SPT" or "Stride Predictor" as shown in Figure 3). As the rejections rely upon the Stride Predictor (not the "Markov prediction table") in asserting correspondence to the claimed invention, this error underpins the impropriety of all claim rejections. This error is exacerbated by the rejections' vague citation to entire sections of the Sherwood reference, without specificity as to the application of specific discussion therein to the alleged correspondence. As Appellant's traversals regarding this matter (as presented in response to the Final Office Action) stand uncontested in the record, Appellant submits that the rejections cannot stand.[1]

As consistent with the above misinterpretation, the Final Office Action has failed to establish correspondence to the claimed invention. For the Board's convenience, Appellant

[1] Appellant notes that, while the Advisory Action alleges that "there appears to be no new arguments" in Appellant's previous response, the above issue was clearly presented yet remains uncontested.

notes that resolution of this issue as presented in Section A(1) below is believed to warrant the reversal of all claim rejections, each of which relies upon the erroneous attribution of functionality to the cited "Stride Predictor." The following addresses these and other improprieties in the rejections in greater detail.

A. The § 102(b) Rejection Over The Sherwood Reference Lacks Correspondence.

1. The § 102(b) Rejection Relies Upon A Misreading Of The Sherwood Reference That Renders All Rejections Improper.

As briefly discussed above, all rejections including the § 102(b) rejection of claims 1-2, 4-8, 10-14, 16-18 and 20 rely upon an asserted correspondence that mistakenly attributes functionality of a Markov prediction table with the cited "Stride Predictor," the latter of which is asserted as corresponding to the "SPT" aspects of the claimed invention. Accordingly, the Final Office Action has not presented any assertion of correspondence that could be used to support the rejections under § 102(b) (or under § 103(a), as addressed in Sections B and C below).

More specifically, as the Examiner has explicitly emphasized that "the Markov Table *is not* the SPT" (emphasis in the Final Office Action), the asserted correspondence is clearly without basis. Because the Examiner acknowledges that "the Markov Table is not the SPT", and there is no other correspondence asserted for the claimed SPT aspects, the rejection is clearly improper. The Office Action cites to section 4.2 in the Sherwood reference as disclosing limitations directed to updating a prediction table only upon on a (cache) miss, and attempts to attribute this functionality to a "Stride Predictor" in the Sherwood reference. However, the cited functionality in the Sherwood reference does not refer to functionality of the "Stride Predictor," and instead refers to functions of a "Markov prediction table." Referring to line 6 of paragraph 2 in section 4.2, the discussed "prediction table" refers back to a "Markov prediction table" at lines 3-4 of the same paragraph, and does not refer back to the "two-delta stride table" (the "Stride Predictor") as asserted in the Office Action. This error is replete throughout all rejections.

In view of the above error, none of the alleged correspondence to the cited "Stride Predictor" is sustainable, as the functionality attributed to the "Stride Predictor" is erroneous.

Accordingly, as all of the § 102(b) rejections rely upon this cited "Stride Predictor" and the erroneously attributed functionality, none of the rejections can stand. Appellant therefore requests that the § 102(b) rejections be reversed, and further notes that the rejections under § 103(a) fail for similar reasons (as also reiterated below).

2. The Final Office Action Failed To Establish Correspondence To Limitations Directed To Limiting Stride Prediction Table Updates To Cache Misses.

The § 102(b) rejection of claims 1-2, 4-8, 10-14, 16-18 and 20 are improper for failing to establish correspondence to aspects of the claimed invention directed to limiting updates to a stride prediction table (SPT), to occur only in response to the detection of a cache miss. In particular (and consistent with the above discussion in Section A(1)), the Final Office Action has asserted that the cited "Stride Predictor" in the Sherwood reference corresponds to aspects of the claimed invention directed to a SPT. However, in an attempt to support the asserted correspondence between the cited "Stride Predictor" and the claimed SPT, the Final Office Action mistakenly refers to the functionality of a Markov "prediction table," and *not* the cited Stride Predictor. Referring to the cited portion of section 4.2 of the Sherwood reference ("[t]he prediction table is only updated on a miss"), the cited portion refers not to the "Stride Predictor," but instead to the "Markov prediction table" as iterated at lines 1-4 of the second paragraph in Section 4.2.

Simply put, the Examiner has mistaken the Sherwood reference's discussion of a "prediction table" as referring to the Stride Predictor. However, the cited "prediction table" refers not to the "Stride Predictor," but to the *Markov* "prediction table." This is consistent with the above introductory discussion regarding these mistaken assertions. Accordingly, the alleged correspondence between the "Stride Predictor" and the claimed SPT is erroneous. Moreover, as the Examiner has explicitly noted that the Markov prediction table does not correspond to the claimed SPT (that "the Markov Table *is not* the SPT" (emphasis in original)), the cited functionality of the Markov prediction table cannot be attributed to the cited Stride Predictor.

Accordingly, the Final Office Action has failed to establish correspondence to aspects of the claimed invention directed to "only allowing updates to the SPT in response to the

detection of a cache miss." As the § 102(b) rejections of all claims rely upon the erroneously asserted correspondence to these aspects, the rejections cannot be maintained. Appellant therefore requests that the rejections be reversed.

3. The Final Office Action Failed To Establish Correspondence To Limitations Directed To Limiting Stride Prediction Table Accesses To Cache Misses.

The § 102(b) rejection of claims 1-2, 4-8, 10-14, 16-18 and 20 are improper for failing to establish correspondence to aspects of the claimed invention directed to limiting accesses to a stride prediction table (SPT), to occur only in response to the detection of a cache miss (*e.g.*, as in claim 1). For example, the cited portions of the Sherwood reference indicating that the "prediction table is only updated on a miss" refer only to a stride update as relevant to the "Stride Predictor," and do not involve restricting other access. Furthermore, the Sherwood reference uses the asserted "prediction table" as part of a prefetching process that will "run ahead" of data streams, and thus does not restrict accesses only to accesses that are responsive to a cache miss. Because of its every-cycle occurrence, this asserted access necessarily occurs at times other than in response to a detected cache miss.

While Appellant has identified the aforesaid errors in its traversals of record, the Examiner has failed to directly address (much less refute) the specific issues at hand. For example, page 11 of the Final Office Action attempts to respond to Appellant's traversals regarding these claim limitations by stating that "the rejections are supported with clarifying comments when a citation alone may be unclear." While the relevance or meaning of this response is unclear, it fails to identify where any correspondence has been asserted to limitations directed to "only allowing accesses to the SPT in response to the detection of a cache miss."

In view of the above, Appellant's repeated traversals of record stand uncontested. Appellant thus submits that the record as it stands is insufficient for maintaining the rejections relying upon the alleged correspondence to limiting SPT access in response to a cache miss. Accordingly, all of the § 102(b) rejections, each of which relies upon these failed assertions of correspondence, are improper. Appellant therefore requests that the rejections be reversed.

4. The Rejections Of Claims 6 And 7 Fail; The Examiner's Allegations Of Inherency Are Unsupported In The Record.

The § 102(b) rejection of claims 6 and 7 are improper for reasons including those as discussed above in Sections A(1)-A(3), and further because the rejections rely upon assertions of allegedly inherent subject matter that are unsupported by any evidence in the record. For example, the Final Office Action fails to establish that the Sherwood reference *necessarily* detects a cache miss as claimed, and fails to provide any evidence supporting the Office Action's assertion that the Sherwood reference "requires" the operation as claimed. As is well known, a cache miss can be detected in a number of ways. For instance, cache misses may involve an instruction read miss, data read miss and data write miss, along with different types of misses within these (*see, e.g.*, Adve *et al.*, "Implementing Sequential Consistency In Cache-Based Systems," *Proceedings of the 1990 International Conference on Parallel Processing*, as cited in the record and which is attached hereto for convenience).

The Office Actions of record have failed to refute the evidence that Appellant's submitted evidence of record (Adve *et al.*), which establishes that a cache miss does not necessarily require the operation as asserted in the rejections. Accordingly the Final Office Action failed to meet the burden under M.P.E.P. § 2131.01(III) in providing intrinsic evidence supporting the alleged inherency and establishing that the cited (Sherwood) reference *necessarily* operates as asserted. Nothing in the record would "make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (emphasis added). Appellant therefore submits that the rejections of claims 6 and 7 are further improper for these reasons, and should be reversed.

B. The § 103(a) Rejection Of Claim 21 Fails To Either Establish Correspondence Or Present Proper Motivation For Combining References.

1. The Rejection Of Claim 21 Fails To Establish Correspondence.

Appellant submits that the § 103(a) rejections of claim 21 fails for lack of correspondence as discussed above regarding the § 102(b) rejections, as applicable here via the Final Office Action's reliance upon the Sherwood reference in the same manner as

applied to other independent claims. These rejections fail because: 1) the Final Office Action mistakenly attributes functionality of a Markov prediction table with the "Stride Predictor," the latter of which is asserted as corresponding to the claimed invention; 2) the assertion that ("[t]he prediction table is only updated on a miss") in the Sherwood reference refers not to the "Stride Predictor" but instead to the "Markov prediction table" as iterated at lines 1-4 of the second paragraph in Section 4.2, failing to establish correspondence to limiting updates to a stride prediction table (SPT); and 3) the asserted correspondence to limiting *accesses* to a stride prediction table (SPT) relies upon a citation to a stride update as relevant to the "Stride Predictor" but does not involve restricting other access, and the asserted "prediction table" is further used in a prefetching process that will "run ahead" of data streams for an every-cycle occurrence (thus does not restrict accesses only to accesses that are responsive to a cache miss).

Appellant further traverses the § 103(a) rejection of claim 21 as, despite Appellant's traversals and requests of record, the Final Office Action failed to point out which portions of the four cited columns correspond to the claimed invention, or aspects of which are asserted as teaching or suggesting respective limitations in claim 21. Instead of providing a clear indication of the asserted correspondence, the Final Office Action asserts that "[s]ince Claim 21 is a method claim, the filter circuit structure is the elements or group of elements which perform the methods of the claimed filter circuit." However, the Final Office Action has not pointed out any such "elements or group of elements which perform the methods of the claimed filter circuit." Any allegations of correspondence to claim 21 are thus incongruous at best, and fail to establish *prima facie* correspondence.

In view of the above, the § 103(a) rejection has failed to establish correspondence to, or teaching or suggestion of, various aspects of the claimed invention as in claim 21. Appellant therefore requests that the rejection of claim 21 be reversed.

2. The Rejection Of Claim 21 Fails To Establish A Proper Reason To Combine The Cited References, Failing To Comply With the 2010 KSR Guidelines.

Appellant further traverses the § 103(a) rejection of claim 21 for reasons similar to those as discussed above in Section B above, as the Final Office Action has again failed to provide a proper reason for combining references, and also attempts to subvert Appellant's traversals without directly addressing the issues presented. In particular, the Final Office Action has failed to provide an explanation as to how the cited SRAM in the (secondary) Matas reference would be combined with the memory in the Sherwood reference, as to where the Matas reference discloses a "single-ported" SRAM, or as to what specific modification of the Sherwood reference is being proposed. Appellant is left to guess as to how these circuits would be (or could be) combined into any hypothetical embodiment that corresponds. The Final Office Action has thus failed to meet the requirements as consistent with the recent U.S.P.T.O. guidelines specifying that "[a]ny rationale employed must provide a link between the factual findings and the legal conclusion of obviousness," and also consistent with the *KSR* decision (cited above) and M.P.E.P. § 2143.01."

More specifically, the Final Office Action fails to provide factual findings regarding any modification of the Sherwood reference, in failing to explain how the Matas reference (*e.g.*, the SRAM TFT cell in Figure 8-10) would be implemented as a single-ported SRAM or would be implemented with the buffer architecture in cited Figure 3 of the Sherwood reference. Moreover, the asserted rationale for combining the references (that SRAM is "commonly used" and is "faster and uses less power") is devoid of any explanation germane to the specific modification at hand, to replace the circuits in the Sherwood reference with the SRAM TFT cell of the Matas reference.

In view of the above, the § 103(a) rejection has failed to present a proper reason for combining references, also failing to meet the requirements as consistent with the recent U.S.P.T.O. guidelines under the *KSR* decision, referenced above. Appellant therefore requests that the rejection of claim 21 be reversed.

C. The § 103(a) Rejection Of Claims 3, 9, 15 And 19 Fails To Establish Correspondence Or Present Proper Motivation For Combining References.

Appellant submits that the § 103(a) rejections of claims 3, 9, 15 and 19 fail for lack of correspondence as discussed above regarding the § 102(b) rejections, as applicable here via the Final Office Action's reliance upon the Sherwood reference as applicable to claims 1, 11 and 17 from which claims 3, 9, 15 and 19 depend. These rejections fail because: 1) the Final Office Action mistakenly attributes functionality of a Markov prediction table with the "Stride Predictor," the latter of which is asserted as corresponding to the claimed invention; 2) the assertion that ("[t]he prediction table is only updated on a miss") in the Sherwood reference refers not to the "Stride Predictor" but instead to the "Markov prediction table" as iterated at lines 1-4 of the second paragraph in Section 4.2, failing to establish correspondence to limiting updates to a stride prediction table (SPT); and 3) the asserted correspondence to limiting *accesses* to a stride prediction table (SPT) relies upon a citation to a stride update as relevant to the "Stride Predictor" but does not involve restricting other access, and the asserted "prediction table" is further used in a prefetching process that will "run ahead" of data streams for an every-cycle occurrence (thus does not restrict accesses only to accesses that are responsive to a cache miss).

Appellant also traverses the § 103(a) rejections of claims 3, 9, 15 and 19 because the Final Office Action fails to provide any explanation or supporting citation as to how the Sherwood reference would function as modified (*e.g.*, fails to present an operable/enabled embodiment establishing a likelihood of success in combining references). Appellant further traverses these § 103(a) rejections as the Final Office Action has not provided any motivation for modifying the Sherwood reference as proposed, thus failing to comply with the requirements detailed in the 2010 USPTO Guidelines under *KSR* regarding establishing obviousness (simply stating that something is obvious or predictable amounts to an unsupported opinion that is insufficient for maintaining a § 103(a) rejection under Guidelines). *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007). In short, the rejections fail to provide an explanation as to how any hypothetical embodiment involving the proposed combination of the Handy and Sherwood references would correspond to the claimed invention, and further rely upon the Examiner's unsupported opinion as to what one

of skill in the art "would recognize" without explaining any nexus between the offered opinion and the combination of references for which the opinion is offered.

Despite Appellant's traversals regarding this matter, the Final Office Action has failed to properly address the issue and instead simply asserts that "these were clearly provided in the previous rejection." Appellant submits that such an assertion is untenable, fails to properly address Appellant's traversals, and further fails provide adequate rationale in the record to support maintaining the rejections. Importantly, Appellant cannot ascertain any such explanation in the record, and the Final Office Action has done nothing to explain where any such explanation was provided. The Examiner's attempt to subvert Appellant's traversals in further asserting that "arguments of counsel cannot take the place of factually supported objective evidence," also fails to address the issue, as Appellant's traversals clearly identified the Final Office Action's failure to explain any relationship between the alleged "motivation" and the proposed combination at hand.

In view of the above, the § 103(a) rejections of claims 3, 9, 15 and 19 have failed to establish correspondence to the claimed invention, and have further failed to meet the requirements for providing motivation/rationale for combining references as asserted under the recent U.S.P.T.O. guidelines and the *KSR* decision. Appellant therefore requests that the § 103(a) rejections be removed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-21 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Respectfully submitted,

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/535,591)

1. A method of data retrieval comprising the steps of:

providing a first memory circuit;

providing a stride prediction table (SPT) that is indexed with cache line miss information;

providing cache memory circuit;

executing instructions for accessing data within the first memory;

detecting a cache miss;

only allowing accesses to the SPT in response to the detection of a cache miss; and

only allowing updates to the SPT in response to the detection of a cache miss.

2. A method according to claim 1 wherein the cache memory circuit is a stream buffer.

3. A method according to claim 1 wherein the cache memory circuit is a random access cache memory.

4. A method according to claim 1 wherein the cache memory circuit and the SPT are within a same physical memory space.

5. A method according to claim 1 wherein the first memory is an external memory circuit separate from a processor executing the instructions.

6. A method according to claim 1 wherein the step of detecting a cache miss includes the steps of determining whether an instruction being executed by the processor is a memory access instruction, when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache; and when the data is other than present within the cache, detecting a cache miss.

7. A method according to claim 1 wherein the step of detecting a cache miss includes the steps of determining whether an instruction to be executed by the processor is a memory access instruction; when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache; and, when the data is other than present within the cache, detecting a cache miss, and accessing and updating the SPT only when the cache miss has occurred.

8. A method according to claim 1, wherein the step of allowing access provides a step of filtering that prevents unnecessary access and updates to entries within the SPT.

9. A method according to claim 1, wherein the cache memory circuit is integral with the processor executing the instructions.

10. A method according to claim 1, wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT.

11. An apparatus comprising: a stride prediction table (SPT) that is indexed with cache line miss information; and, a filter circuit for use with the SPT, the filter circuit preventing both accesses and updates to the SPT unless a cache miss is detected.

12. An apparatus according to claim 11 comprising a memory circuit, the memory circuit for storing the SPT therein.

13. An apparatus according to claim 12 comprising a cache memory, the cache memory residing within the memory circuit.

14. An apparatus according to claim 13, wherein the memory circuit is a single ported memory circuit.

15. An apparatus according to claim 13, wherein the memory circuit is a random access memory circuit.

16. An apparatus according to claim 11, wherein the cache memory circuit is a stream buffer.

17. A method of data retrieval comprising the steps of:

providing a first memory circuit;

providing a stride prediction table (SPT) that is indexed with cache line miss information;

providing cache memory circuit;

executing instructions for accessing data within the first memory;

detecting a cache miss; and

restricting accesses to the SPT in response to the detection of a cache miss.

18. A method according to claim 17, wherein the step of restricting provides a step of filtering that prevents unnecessary access and updates to entries within the SPT.

19. A method according to claim 17, wherein the cache memory circuit is integral with the processor executing the instructions.

20. A method according to claim 17, wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT.

21. A method of data retrieval, the method comprising:

providing a first memory circuit;

providing a single-ported SRAM memory having a cache memory circuit and a stride prediction table (SPT) that is indexed with cache line miss information;

in a filter circuit,

receiving an application stream having a plurality of access instructions for accessing data in the first memory circuit,

for each of the plurality of access instructions that are load access instructions,

accessing the cache memory to determine whether data at a memory location of the load access instruction is present within the cache, and

when the data is other than present within the cache, detecting a cache miss for the load access instruction,

restricting accesses and updates to the SPT to only load memory access instructions for which a cache miss is detected;

in response to an update to the SPT indicative of one of said detected cache misses, executing instructions to access the SPT and predict a cache miss; and

in response to a predicted cache miss, control the loading of a stream cache based upon the memory location of the load access instruction.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.